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The Ferroelectric Field Effect within an Integrated Core/Shell Nanowire

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The synthesis of cylindrical silicon-core and ferroelectric oxide perovskite-shell nanowires and their response characteristics as individual three-terminal nanoscale electronic devices is reported. The co-axial nanowire geometry facilitates large ferroelectric field-effect modulation ($>10^4$) of nanowire conductivity following sequential application and removal of an applied dc field. Source-drain current–voltage traces collected during sweeps of ferroelectric gate potential and switching of the component of shell outward and inward polarization provide direct evidence of ferroelectric coupling on nanowire channel conductance. Despite a very small (1:20) ferroelectric-to-semiconductor channel thickness ratio, an unexpectedly strong electrostatic coupling of ferroelectric polarization to channel conductance is observed because of the co-axial gate geometry and curvature-induced strain enhancement of ferroelectric polarization.

1. Introduction

Among modes of non-volatile (NV) memories, ferroelectric random access memories (FeRAMs) are distinguished by lower power consumption, faster write performance, a many orders of magnitude higher maximum number of write-read cycles, and radiation-hard operation.[1] Despite these advantages, the practical scalability of FeRAMs to current node sizes is constrained primarily by a minimum charge associated with the ferroelectric capacitor required to trigger a sensing amplifier, and by the effects of an internal depolarizing field.[2–6] Ferroelectric-based NV memories include those based on tunneling electroresistance, tunneling electromagnetoresistance, and the ferroelectric field effect using a metal-ferroelectric-semiconductor (MFS) structure,[7] in which the gate oxide of a metal-oxide-semiconductor (MOS) structure is replaced by a ferroelectric oxide. In the ferroelectric field-effect transistor (FeFET) non-volatile writing and non-destructive readout is achieved via modulation

of carrier transport in the adjacent semiconductor channel.[8,9] FeFETs have been realized mainly in two device geometries: ferroelectric films with thin-film channels,[7,10–13] including also graphene[14]; and ferroelectric films with nanoscale channels, including, e.g., a semiconducting nanowire (NW)[15,16] or carbon nanotube.[17] In these and related field-effect devices, the ferroelectric gate oxide thicknesses (~100 – 500 nm) are two orders of magnitude larger[7,15,16,18] than that for the state-of-the-art node.

Here we report on the synthesis and functionality of integrated ferroelectric/semiconductor nanostructures exhibiting ferroelectric field effect modulation of a semiconductor channel. The NWs, each consisting of a Si core and a $PbZr_{0.52}Ti_{0.48}O_3$ (PZT) ferroelectric shell, are produced using a combination of template-assisted synthesis of ferroelectric nanotubes and chemical vapor deposition (CVD) of Au-catalyzed Si NWs. The core-shell NWs each possess an electrical contact to the Si core near the ends, and one or more contacts on the PZT shell. The NW cores exhibit a nearly 10^5 decrease in current within the Si NW core following application and removal of a gate voltage. The observed ferroelectric field-effect in this intrinsically sub-micrometer structure involves manipulation of ferroelectric polarization within the shell having a component oriented preferentially in the shell outward or inward normal direction.[19] This functionality in a heterostructure having small ferroelectric-to-semiconductor channel thickness ratio (1:20) is enabled by the core-shell geometry, and by effect of curvature-driven strain and associated polarization gradient on ferroelectric stability.[19]

2. Results and Discussion

A sequence of template-assisted sol-gel synthesis and crystallization,[20–22] metal evaporation, electrodeposition, CVD,[23] template dissolution and electron beam lithography was developed to produce electrically interfaced Si-core, ferroelectric PZT shell NWs (**Figure 1** and Experimental Section). Plotted in **Figure 2**b is a representative series of Si NW current-bias voltage traces collected from one of these structures (Figure 2a) after the application and removal of selected values of gate voltage ($g_1 = 1.0$ V $\leq V_g \leq 9.0$ V, -11 V; $g_1 = 3$ V, $g_2 = -15$ V) as denoted in

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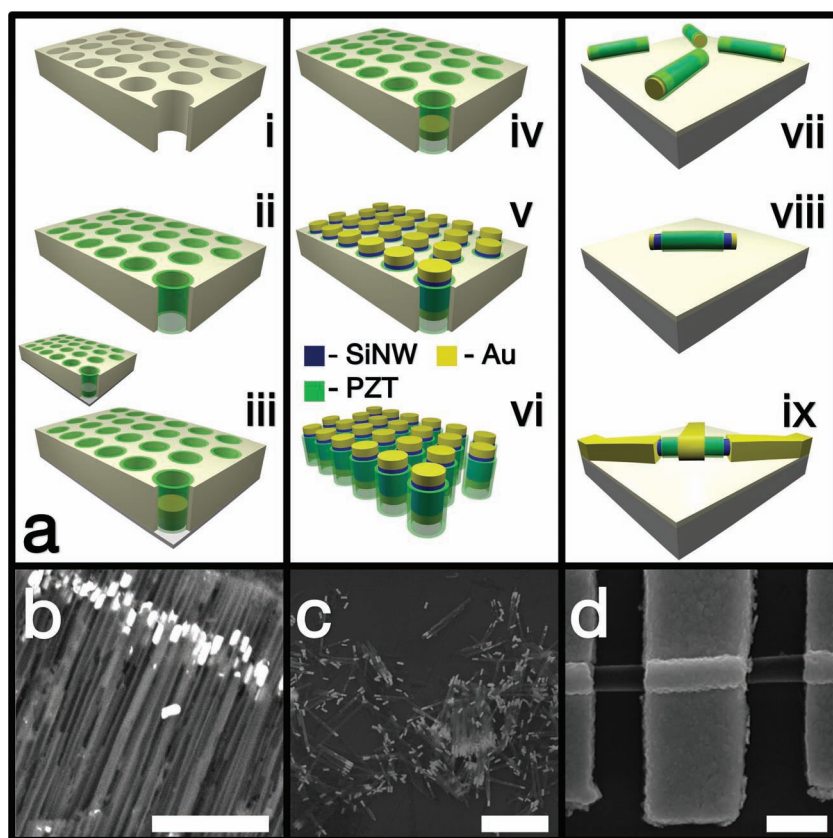University of Pennsylvania, Philadelphia, PA 19104

Figure 1. a) Schematic of the Si-PZT core/shell synthesis process: i) bare anodic aluminum oxide (AAO) template, ii) wetting of pores with PZT metallic alkoxide sol-gel precursor, iii) thermal evaporation of Ag as back electrode and electrochemically reduced Ag NW support segment (inset) and Au NW catalyst segment, iv) selective etching of Ag backcoating and support segment, v) growth of SiNWs within PZT nano-shells *via* CVD using diluted SiH$_4$, vi) selective dissolution of the AAO template (color legend denotes materials within core-shell), vii) dispersion of freestanding NWs on a SiO$_2$/Si wafer, viii) lithographic patterning of windows on NWs ends via registered EBL and selectively etch the shell from the core, and ix) thermal evaporation of metallic electrodes to produce electrically addressable NW core. b) SEM image of Si-core, PZT-shell NWs as grown in the AAO template (scale: 5 μm); c) SEM image of Si-core, PZT-shell NWs dispersed on a SiO$_2$/Si wafer (scale: 10 μm); d) SEM image of gated Si-core, PZT-shell NW (scale: 1 μm). Unlike conventional VLS growth of NWs, where the catalyst particle is supported by a substrate surface, template-directed VLS growth[23] uses catalyst particles buried deep within individual pores (panel (a), iv). This allows the process gas (SiH$_4$) to diffuse within the pore and react on both sides, typically resulting in metal catalyst caps on each end of the produced nanowire, as illustrated in panel (a),v.

the legend. Strong remnant coupling of gate voltage to the NW channel conductance is seen, similar to that observed in NWs obtained using planar ferroelectric thin films.[15,16] Remarkably, the gating achieved by the ≈10-nm thick PZT cylindrical shell produces more than an order of magnitude difference in source-drain current I_{sd} following application and removal of V_g = 1.0 V, and more than two orders of magnitude difference following application and removal of V_g = 9.0 V.

The measured current traces following application and removal of V_g = 9.0 V and then a negative gate voltage V_g = −11.0 V do not appear to change significantly. However, the subsequent application and removal of a positive gate voltage V_g = 3.0 V to two gate electrodes together (approximately doubling the effective gate area, Figure 2a) produces another two

orders of magnitude reduction in the current, and the application and removal after that of a negative gate voltage (V_g = −15.0 V) results in an increase (i.e., partial recovery) of more than an order of magnitude suggests the importance of gate electrode area to the effectiveness of ferroelectric coupling to the NW channel. While one might expect the application and removal of large negative gate voltages to result in a very different response, possibly in an enhancement of the conduction, and the subsequent application of a positive gate voltage to produce a recovery, we do observe a strong effect with larger gate area and polarity. The absence of a recovery of the current values following application and removal of large values of gate voltage can be due to the low conductivity of the SiNW, particularly following application and removal of gate voltages that reduce the SiNW conductance: with application and removal of progressively larger gate voltages, the region over which the electric field drops–assumed to be primarily across the ferroelectric–is extended to the entire nanowire to its drain contact, thereby reducing significantly the actual magnitude of the field. Nevertheless, the current suppression (from the as-found state) of nearly five orders of magnitude is comparable if not exceeding that reported for state-of-the-art FeFETs[24] which involves much larger devices. To quantify the gating effectiveness of the PZT wrap-gate we estimate the inverse sub-threshold swing S = ln 10 dV_g/d($ln I_{sd}$) of the device using the data in Figure 2b (noting that this is not a metric that is normally applicable to ferroelectric memories). Using the data obtained with the single-electrode gate (g_1), S ≈ 430 mV/dec (Figure 2b). When the larger gate area is used (3/4 of the channel length via g_1 and g_2) S < 350 mV/dec., comparable to that reported for planar FeFET devices.[15]

The ferroelectric origin of the observed orders-of-magnitude difference in NW core channel conductance was confirmed by collecting I_{sd} as a function of V_g using a modified NW structure. Si-core and PZT-shell NWs were prepared with the introduction of a ≈20-nm thick HfO$_x$ dielectric buffer layer situated between the gate metal electrode and the PZT shell in order to reduce the leakage current through the PZT shell (Experimental Section), producing an integrated NW-based metal-oxide-ferroelectric-semiconductor (MOFS) device. Shown in **Figure 3**b is an electron microscopy image of a gated Si-core, PZT-shell NW possessing the HfO$_x$ dielectric buffer shell layer (pink region in illustration in the lower portion of Figure 3b). The collected source-drain current of the structure (Figure 3b) under sweeping gate voltage (±10 V) and fixed source-drain bias V_b = 2.0 exhibits hysteresis (Figure 3c),
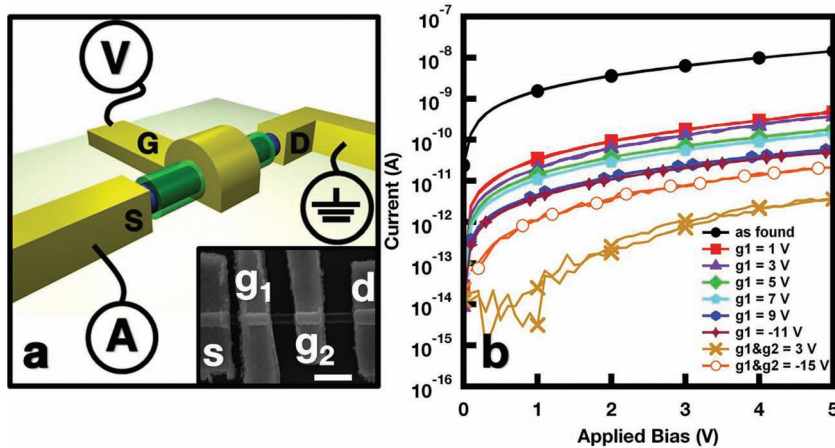
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Figure 2. a) Schematic for collection of source-drain current-bias voltage (I_{sd}–V_b) following application and removal of gate voltages (V_g) involving an individual Si-core, PZT-shell NW. Inset: SEM image of a core/shell NW possessing a split-gate, with source (*s*), drain (*d*), left-gate (g_1), and right-gate (g_2) denoted, scale = 1 μm. b) Log scale plot of the collected I_{sd}–V_b response showing the effect of gating of the PZT-shell after application (and removal) of different values of V_g to gate electrode denoted by g_1 and g_1 and g_2, including the collected response prior to application of any gate voltage (black filled circles), indicating strong dependence on V_g. A more than four orders of magnitude decrease from the as-found NW current following application and removal of V_g = 3 V to both g_1 and g_2 simultaneously is observed.

and the current values did not decrease or increase significantly after ≈12 h. Significantly, the source-drain current I_{sd}–V_g trajectory of the hysteresis is anti-clockwise, consistent with previous reports involving thin film FeFETs and with an n-type character[15] of the present NW channel.

The ferroelectric field-induced variation of I_{sd}(≈0.1 pA) during switching in the MOFS structure is small in relation to MFS structures involving semiconductor NWs and planar ferroelectric films.[15] However its observation is noteworthy when one considers the thickness of the ferroelectric shell (≈10 nm) in comparison to ferroelectric layer thicknesses in planar FeFETs and in planar-ferroelectric film/NW channel device (≈100 − 500 nm).

The ferroelectric/semiconductor thickness ratio is an important consideration for scalability. The thickness ratio for the present core-shell NWs (1:20) is 800 times smaller than that for the planar PZT film gate/In$_2$O$_3$ NW channel (40:1).[15] We also note that for the co-axially gated NW geometry the capacitance of the MFS structure can be estimated using[25]

$$ C = \frac{2\pi \epsilon_o \epsilon_{PZT} L}{\ln \left(1 + 2t_{PZT}/d_{nw}\right)} \tag{1} $$

Here L(= 1 μm) is the channel length, t_{PZT}(= 10 nm) the thickness of the ferroelectric oxide layer, and d_{nw}(= 200 nm) the diameter of the semiconducting NW channel. With ε_{PZT} (= 400),[16] C = 0.23 pF, comparable to non-ferroelectric NW capacitances and considerably smaller than for the NW channel and thicker, planar ferroelectric gate oxide films (≈10^2 pF).[15,16] In addition, mitigation of short-channel effects is an important consideration in achieving efficient coupling of gate voltage throughout the channel, through the so-called

natural length of the NW channel λ, which also depends on the aforementioned thickness ratio.[26] For the present MFS NW case,

$$ \lambda = \sqrt{\frac{2\epsilon_{Si} d_{nw}^2 \ln \left(1 + \frac{2t_{ox}}{d_{nw}}\right) + \epsilon_{ox} d_{nw}^2}{16\epsilon_{ox}}} \tag{2} $$

where ϵ_{Si} = 11.7 is the dielectric constant of the Si NW channel, λ ≈ 50 nm, within an order of magnitude of that for planar ferro-electric-semiconductor NW systems.[16] The integrated PZT-Si NW system presented here also satisfies the gate length requirement of $L_g > 4.6\lambda$ necessary to limit short channel effects and maximum potential control.[26]

3. Conclusion

The findings associated with the present NW-based model system suggest how a three-dimensional nanoscale structure[27] that incorporates ferroelectric gates can be used to overcome limitations posed by inherently two-dimensional ferroelectric structurestews.[7,18] Improvements in performance and functionality may be realized through selection of ferroelectric and dielectric shell combinations, smaller core diameter and higher doping, multiple and individually addressable gates and associated states. The application to integrated semiconductor-ferroelectric NWs of processes developed for the transfer of semiconductor NWs onto a range of different substrates and their electrical interfacing can create a more flexible design platform for ferroelectric memories. We anticipate that the versatility of the modular synthetic approach reported here will permit facile preparation and study of multi functional properties (i.e.; ferromagnetic, multiferroic, magnetoelastic) of NWs composed of other combinations of material,[28] including other semiconductor and complex oxide materials.

4. Experimental Section

PZT ferroelectric shells were synthesized via pore wetting of commercial (Whatman Anodisc 200) anodized aluminum oxide (AAO) templates (Figure 1 (i-ii9) using a commercially available polymeric sol-gel precursor (Chemat PZT9103). Nanotube-embedded templates were back-coated with a 100-nm thick thermally-evaporated layer of Ag using resistive thermal evaporation (Figure 1a (iii)), facilitating its use as a working electrode for galvanostatic reduction of Ag and Au, sequentially, to produce segments of Ag (≈10 μm; 100 μA; 2 h) and Au (≈200–500 nm; 70 μA; 20 min; Figure 1a (iii)). The AgNW segments ensure the Au catalyst segments are well supported (and embedded) within the PZTNT, allowing SiNW growth within the ferroelectric nanotube. After a <5 min selective etch of the Ag film and nanosegments in 8 M HNO$_3$ Au catalyst segments (Figure 1a iv) were used to catalyze the growth of Si NWs within the templates using CVD under vapor-liquid-solid conditions (Figure 1a (v)).[23]
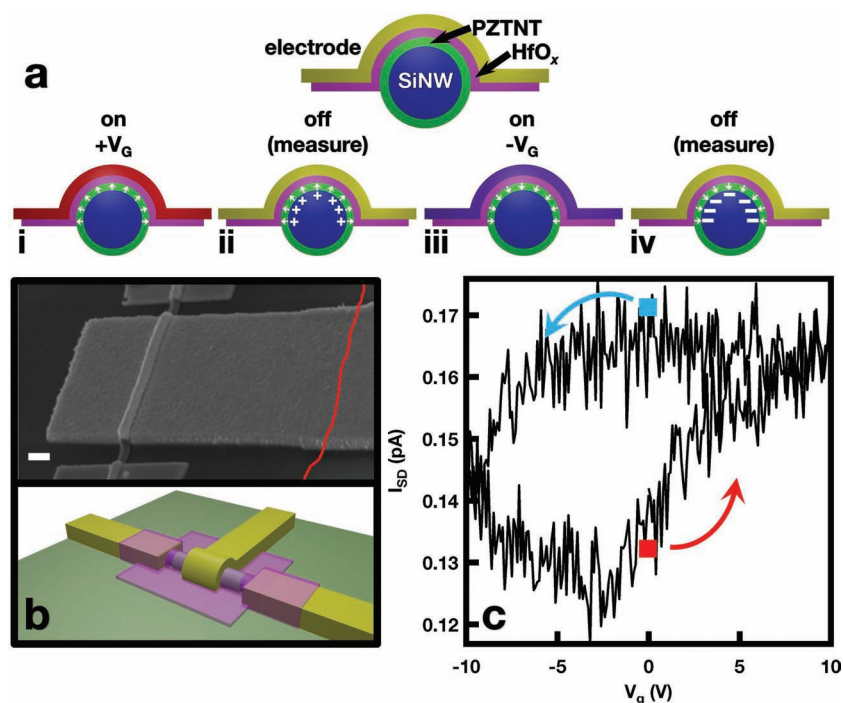
Figure 3. a) Idealized schematic of the Si nanowire channel within the PZTNT i) during application of positive gate voltage, ii) under the influence of the remnant ferroelectric field effect (after voltage is removed), iii) during application of negative gate voltage, and iv) under the influence of the remnant ferroelectric field effect (after voltage is removed). This simplified schematic ignores surface and interfacial trap charge considerations. b) Top: SEM image of the metal-oxide-ferroelectric-semiconductor NW device (hafnia region begins at red line), scale = 1 μm. Bottom: illustration of MOFS structure showing location of HfO_x dielectric (pink region). c) Collected source-drain current vs. V_g for an individual Si core, PZT inner shell, and HfO_x outer shell NW; $V_b = 2$ V. The red and light blue squares indicate the distinct current states found at $V_g = 0$ V, the arrows indicate the anti-clockwise direction of the current under the applied bias sweep The inclusion of the HfO_x significantly reduces the leakage, and thereby permits measurement of the effect of variation of gate voltage on the conductance of the SiNW owing to the thin ferroelectric shell, and therefore a validation of the ferroelectric mechanism.

(Cambridge Nanotech; Savannah 100) using a precursor consisting of tetrakis(dimethylamido) hafnium (Aldrich) and deionized water. The precursors were injected into the reactor and held at 200 °C separately, with each injection followed by a 10 s pulse of ultrahigh purity nitrogen purge gas flowing at 20 sccm. The process consisted of 200 precursor/oxidant at a film growth rate of 1 Å/cycle, leading to the final HfO_x film thickness of ≈20 nm.

All measurements were collected under vacuum (10^{-6} torr) using a picoammeter (Keithley 6487) for collection of I_{sd} and a source meter and electrometer (Keithley 2400; Keithley 617) for application of V_g. The measurement sequence for each NW involved i) grounding of the gate voltage ($V_g = 0$) using the probe followed by retraction of the probe; ii) collection of I_{sd} for the NW under floating gate potential (probe retracted); iii) placement of probe on the gate electrode, and application of one value of selected gate bias ($V_g > 0$) for ≈2 min followed by reduction of gate bias to $V_g = 0$ for ≈2 min prior to lifting the probe; and iv) collection of I_{sd} for the NW under floating gate potential (probe retracted); and repetition of steps (iii) and (iv) for each of the selected values of V_g.

Nanotube and catalyst segment embedded templates were loaded into a quartz furnace tube and heated to 500 °C under the flow of H_2 (50 standard cubic centimeters (sccm)) at a base pressure of 13 torr. SiH_4 (5% in H_2) (Airgas Corporation) was then introduced (50 sccm) for 1 h, resulting in growth of SiNWs within the PZT nanotubes (Figure 1b). Samples were then cooled under flow of H_2 (50 sccm) to room temperature, followed by selective etching of the AAO using 6 M NaOH, resulting in a solution of freestanding Si-core, PZT-shell NW (Figure 1a (vi) and Figure 1c). The isopropanol-based solutions of NWs were then dispersed onto a pre-patterned SiO_2/Si wafer (Figure 1a (vii)), selective wet etching (Figure 1a (viii)) of the PZT shell was used to open up windows for metallization and finally Cr (10 nm) and Au (150 nm) were thermally-evaporated through the windows, thereby permitting addressable NW inner electrodes (Figure 1a (ix) and Figure 1d).

To produce the integrated metal-oxide-ferroelectric semiconductor (MOFS) test structures, samples containing source-drain contacted NWs were coated in electron-sensitive 950K molecular weight poly-methyl methacrylate (PMMA) resist (MicroChem; Newton, MA) following which electron-beam lithography was used to pattern large square pads over the area between the electrically contacted NW ends. A thin layer (<20 nm) of HfO_x was then deposited via atomic layer deposition

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